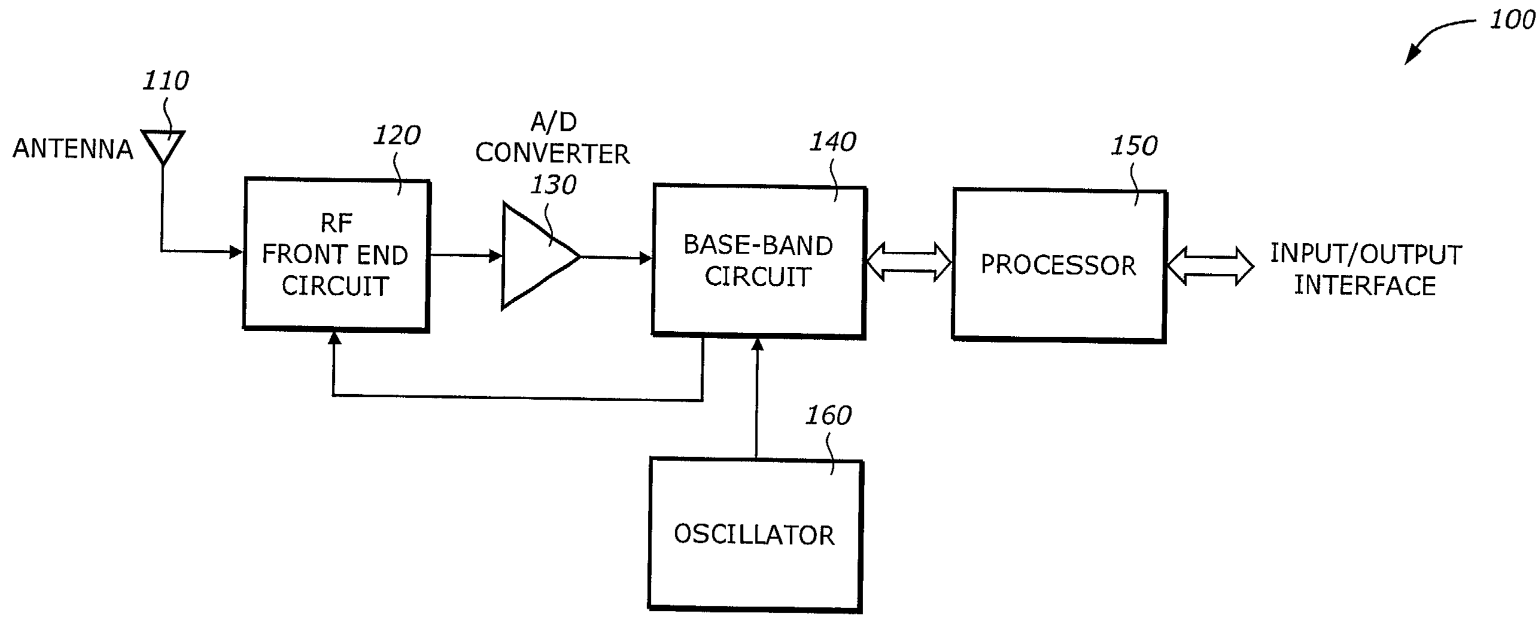
100
110
ANTENNA
120
RF
FRONT END
CIRCUIT
A/D
CONVERTER
130
140
BASE-BAND
CIRCUIT
150
PROCESSOR
INPUT/OUTPUT
INTERFACE
160
OSCILLATOR

FIG. 1

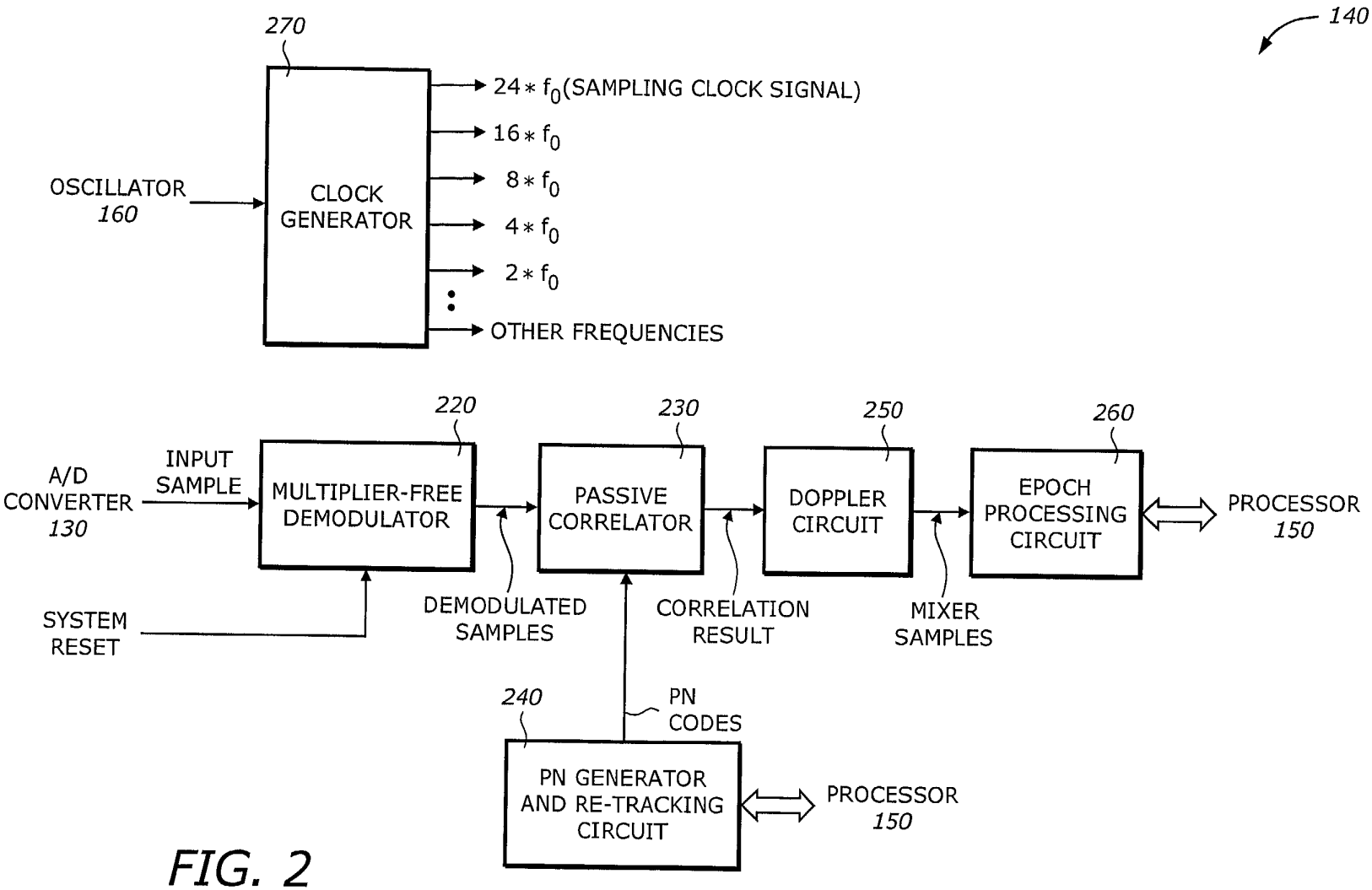
140
270
24 * f0 (SAMPLING CLOCK SIGNAL)
16 * f0
8 * f0
4 * f0
2 * f0
OTHER FREQUENCIES
OSCILLATOR
160
CLOCK GENERATOR
220
230
250
260
A/D CONVERTER
130
INPUT SAMPLE
MULTIPLIER-FREE DEMODULATOR
PASSIVE CORRELATOR
DOPPLER CIRCUIT
EPOCH PROCESSING CIRCUIT
PROCESSOR
150
SYSTEM RESET
DEMODULATED SAMPLES
CORRELATION RESULT
MIXER SAMPLES
240
PN CODES
PN GENERATOR AND RE-TRACKING CIRCUIT
PROCESSOR
150

FIG. 2

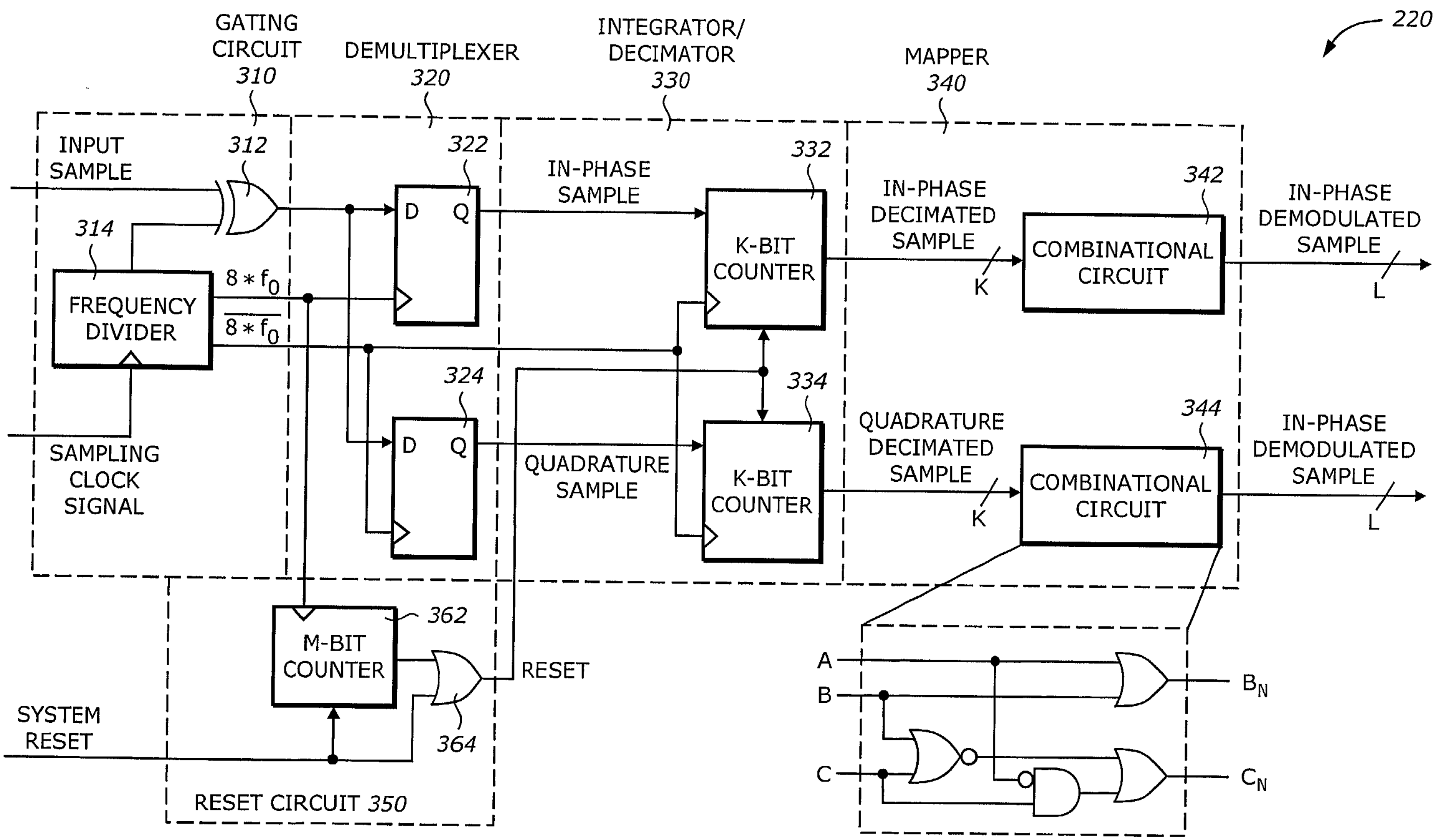
220
GATING CIRCUIT 310
DEMULTIPLEXER 320
INTEGRATOR/ DECIMATOR 330
MAPPER 340
INPUT SAMPLE
312
314
FREQUENCY DIVIDER
SAMPLING CLOCK SIGNAL
8 * f0
8 * f0
322
D Q
324
D Q
IN-PHASE SAMPLE
QUADRATURE SAMPLE
332
K-BIT COUNTER
334
K-BIT COUNTER
IN-PHASE DECIMATED SAMPLE
QUADRATURE DECIMATED SAMPLE
K
K
342
COMBINATIONAL CIRCUIT
344
COMBINATIONAL CIRCUIT
IN-PHASE DEMODULATED SAMPLE
IN-PHASE DEMODULATED SAMPLE
L
L
362
M-BIT COUNTER
364
RESET
SYSTEM RESET
RESET CIRCUIT 350
A
B
C
BN
CN

FIG. 3

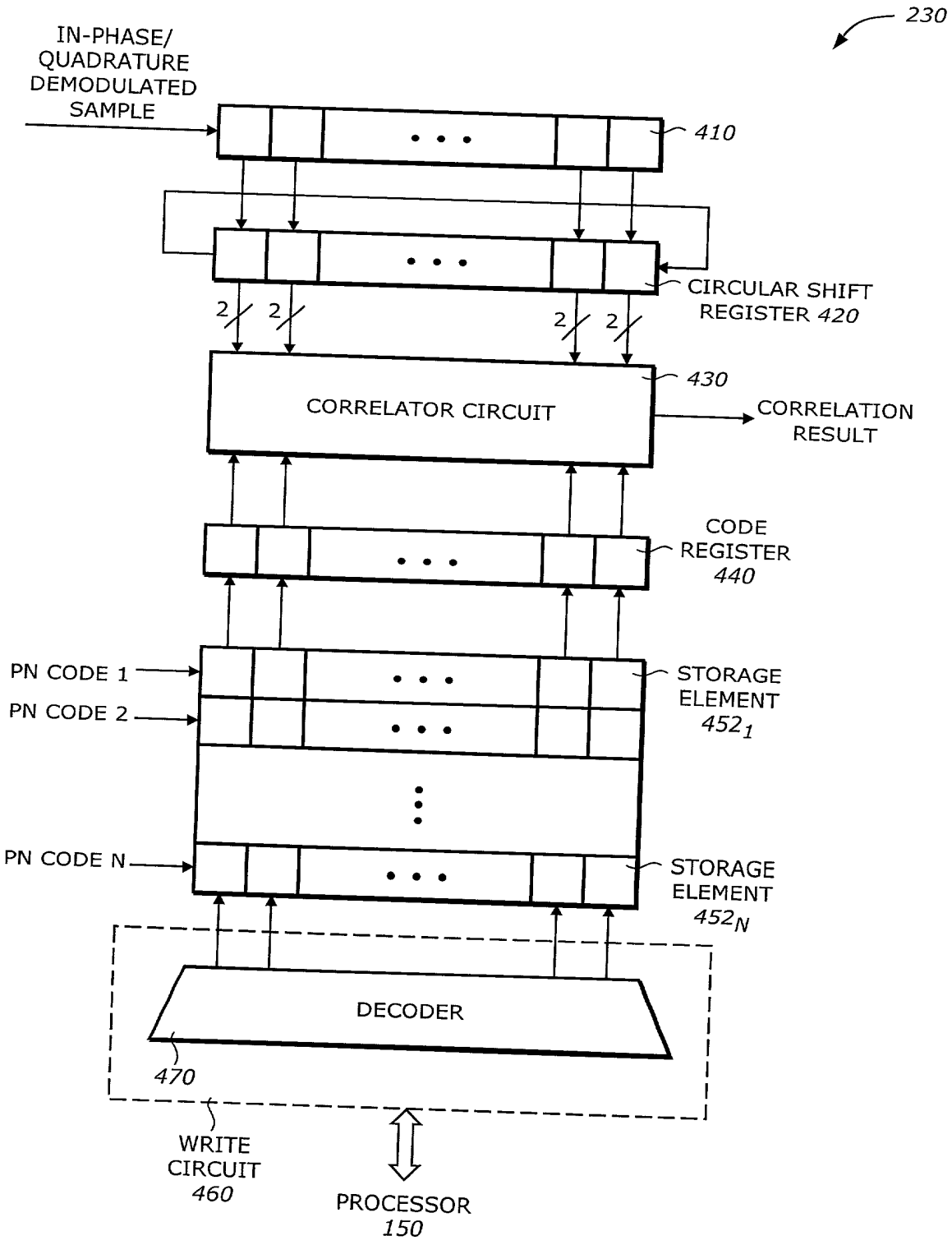
230
IN-PHASE/
QUADRATURE
DEMODULATED
SAMPLE
410
CIRCULAR SHIFT
REGISTER 420
2
2
2
2
430
CORRELATOR CIRCUIT
CORRELATION
RESULT
CODE
REGISTER
440
PN CODE 1
PN CODE 2
PN CODE N
STORAGE
ELEMENT
452_1
STORAGE
ELEMENT
452_N
DECODER
470
WRITE
CIRCUIT
460
PROCESSOR
150

FIG. 4

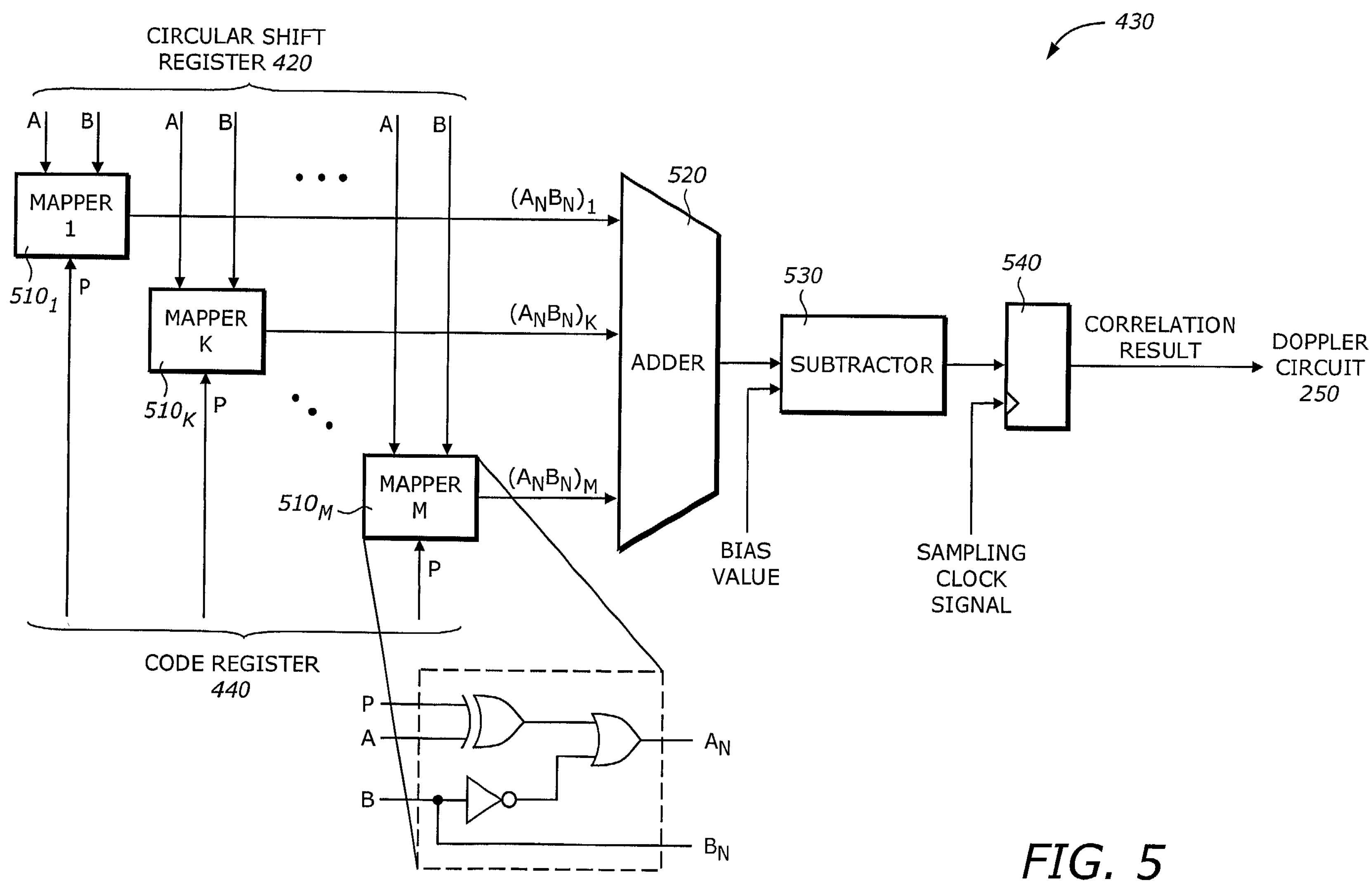
430
CIRCULAR SHIFT REGISTER 420
A
B
MAPPER 1
510_1
P
MAPPER K
510_K
MAPPER M
510_M
CODE REGISTER 440
$(A_N B_N)_1$
$(A_N B_N)_K$
$(A_N B_N)_M$
520
ADDER
530
SUBTRACTOR
BIAS VALUE
540
SAMPLING CLOCK SIGNAL
CORRELATION RESULT
DOPPLER CIRCUIT 250
A_N
B_N

FIG. 5

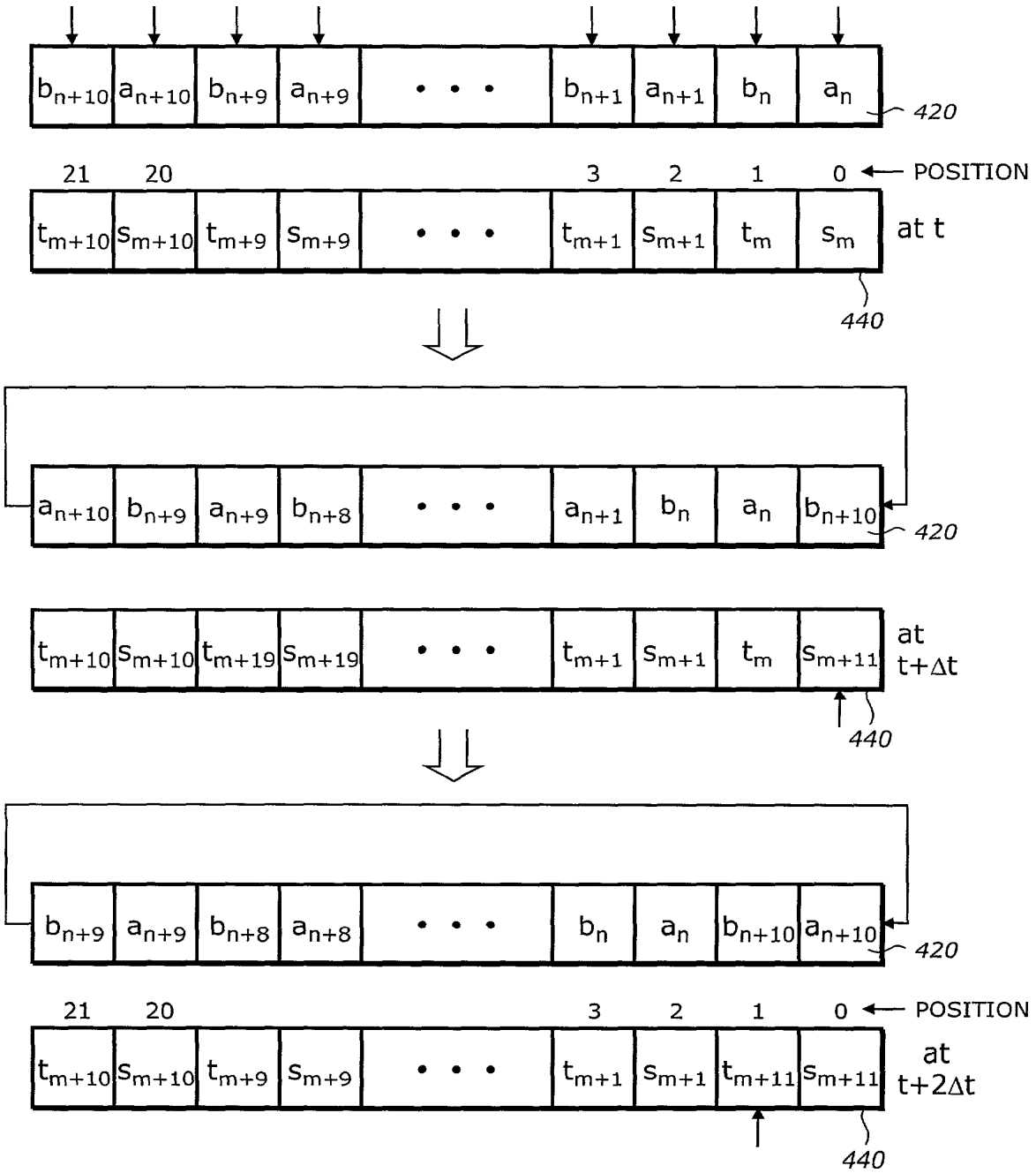
b_{n+10} a_{n+10} b_{n+9} a_{n+9} • • • b_{n+1} a_{n+1} b_n a_n
420
21 20 3 2 1 0
POSITION
t_{m+10} s_{m+10} t_{m+9} s_{m+9} • • • t_{m+1} s_{m+1} t_m s_m
at t
440
a_{n+10} b_{n+9} a_{n+9} b_{n+8} • • • a_{n+1} b_n a_n b_{n+10}
420
t_{m+10} s_{m+10} t_{m+19} s_{m+19} • • • t_{m+1} s_{m+1} t_m s_{m+11}
at t+Δt
440
b_{n+9} a_{n+9} b_{n+8} a_{n+8} • • • b_n a_n b_{n+10} a_{n+10}
420
21 20 3 2 1 0
POSITION
t_{m+10} s_{m+10} t_{m+9} s_{m+9} • • • t_{m+1} s_{m+1} t_{m+11} s_{m+11}
at t+2Δt
440

FIG. 6

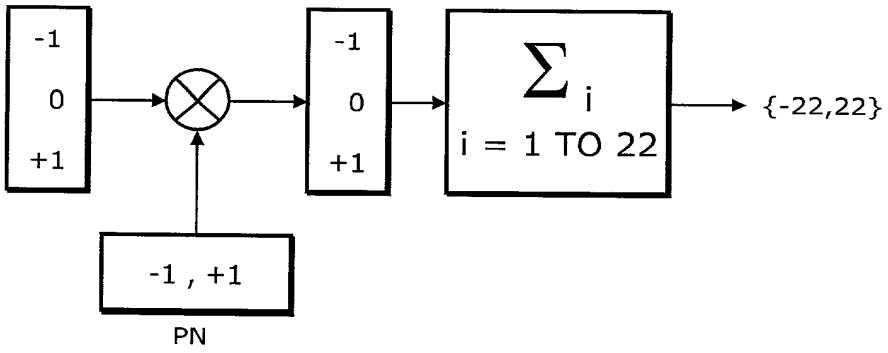

FIG. 7A

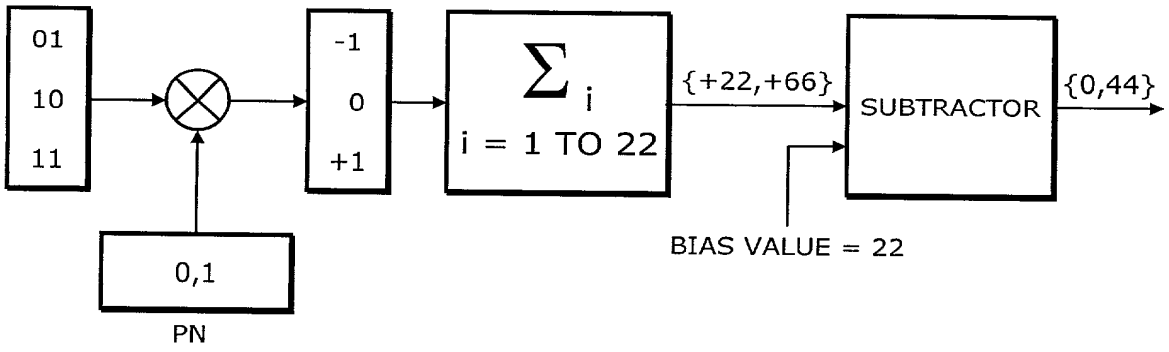

FIG. 7B

PN CODE

DATA SAMPLES	0	1
01	01	11
10	10	10
11	11	01

FIG. 7C

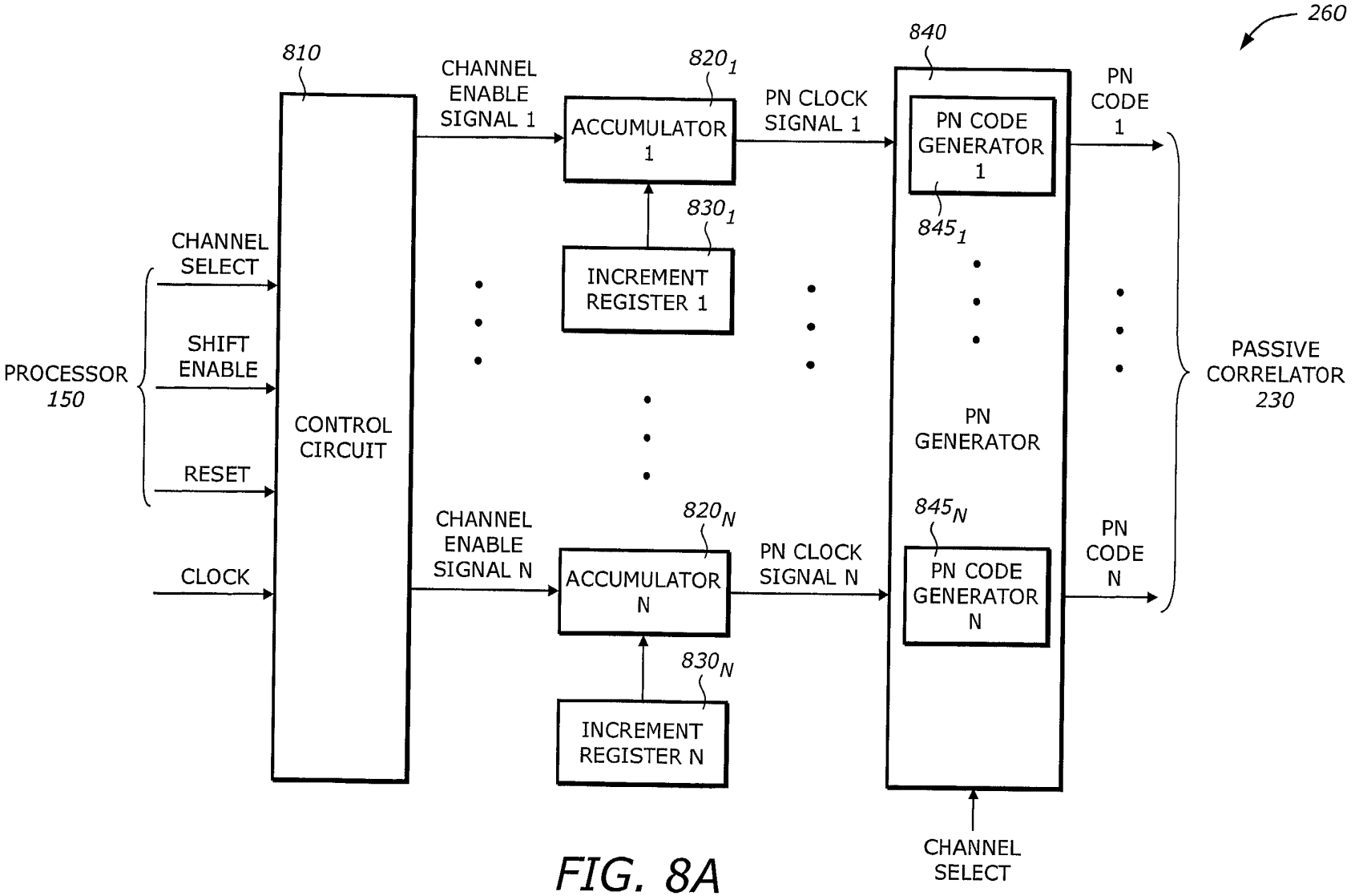

FIG. 8A

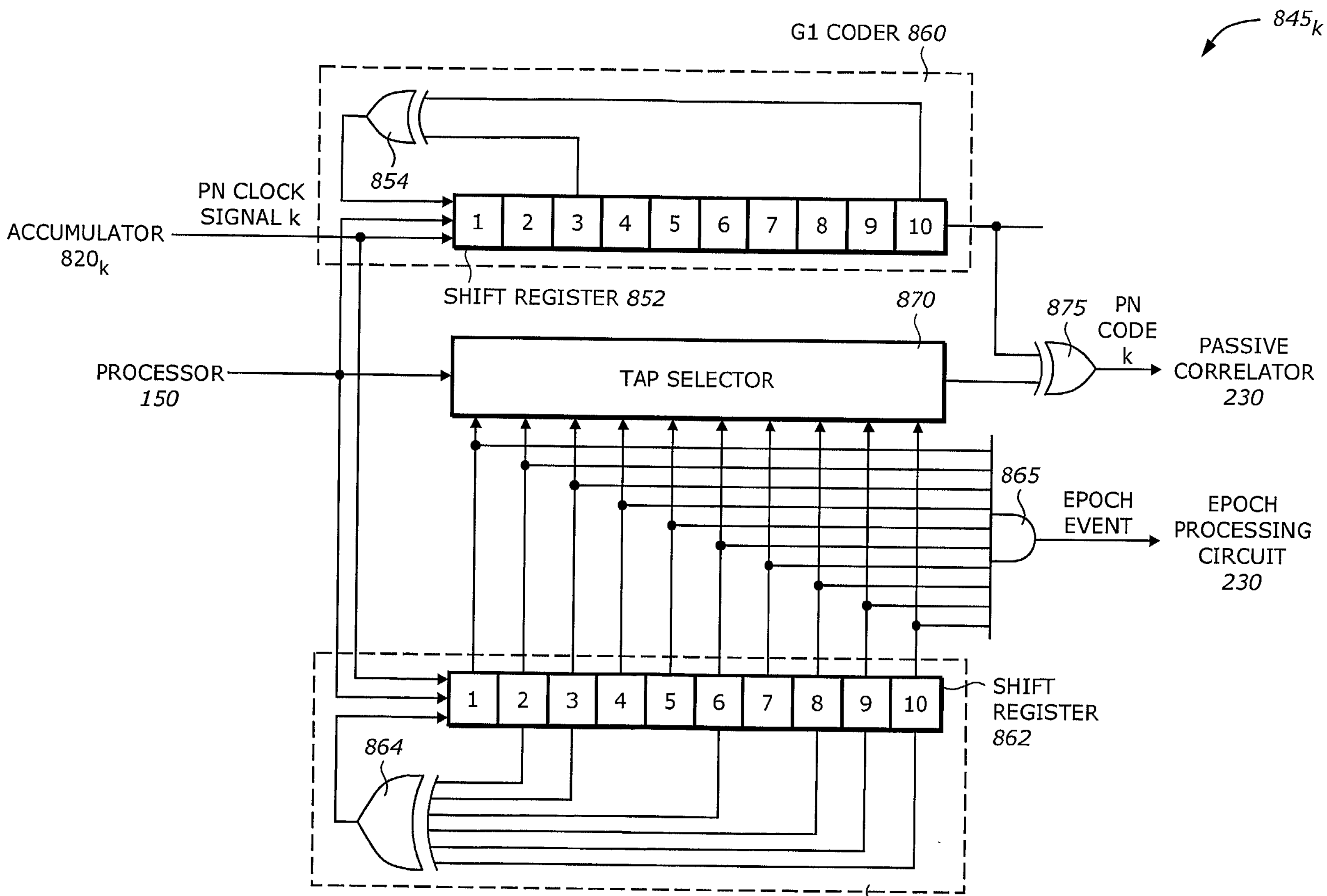
845k
G1 CODER 860
854
PN CLOCK SIGNAL k
ACCUMULATOR 820k
1 2 3 4 5 6 7 8 9 10
SHIFT REGISTER 852
870
TAP SELECTOR
PROCESSOR 150
875
PN CODE k
PASSIVE CORRELATOR 230
865
EPOCH EVENT
EPOCH PROCESSING CIRCUIT 230
1 2 3 4 5 6 7 8 9 10
SHIFT REGISTER 862
864
G2 CODER 860

FIG. 8B

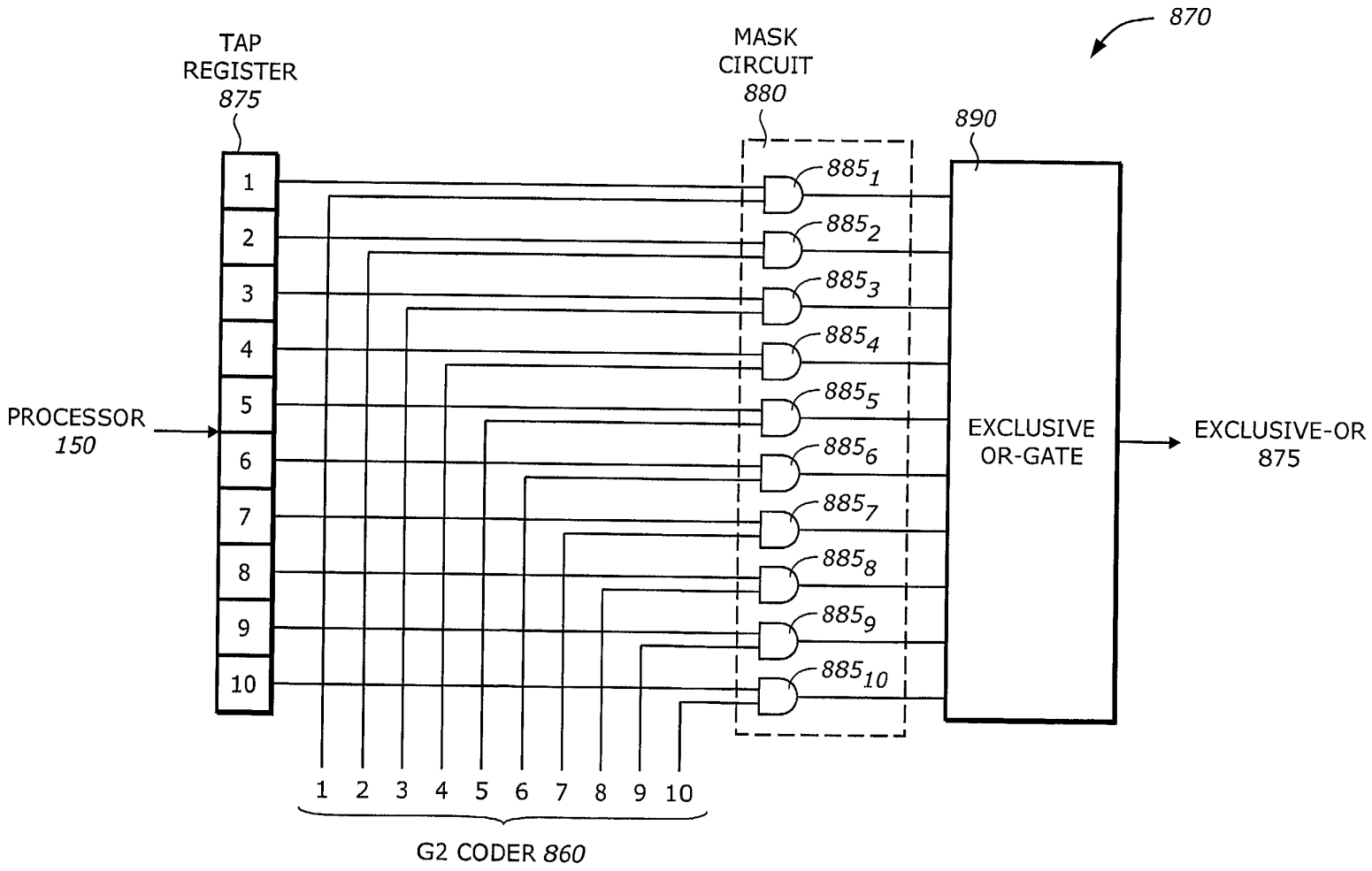

FIG. 8C

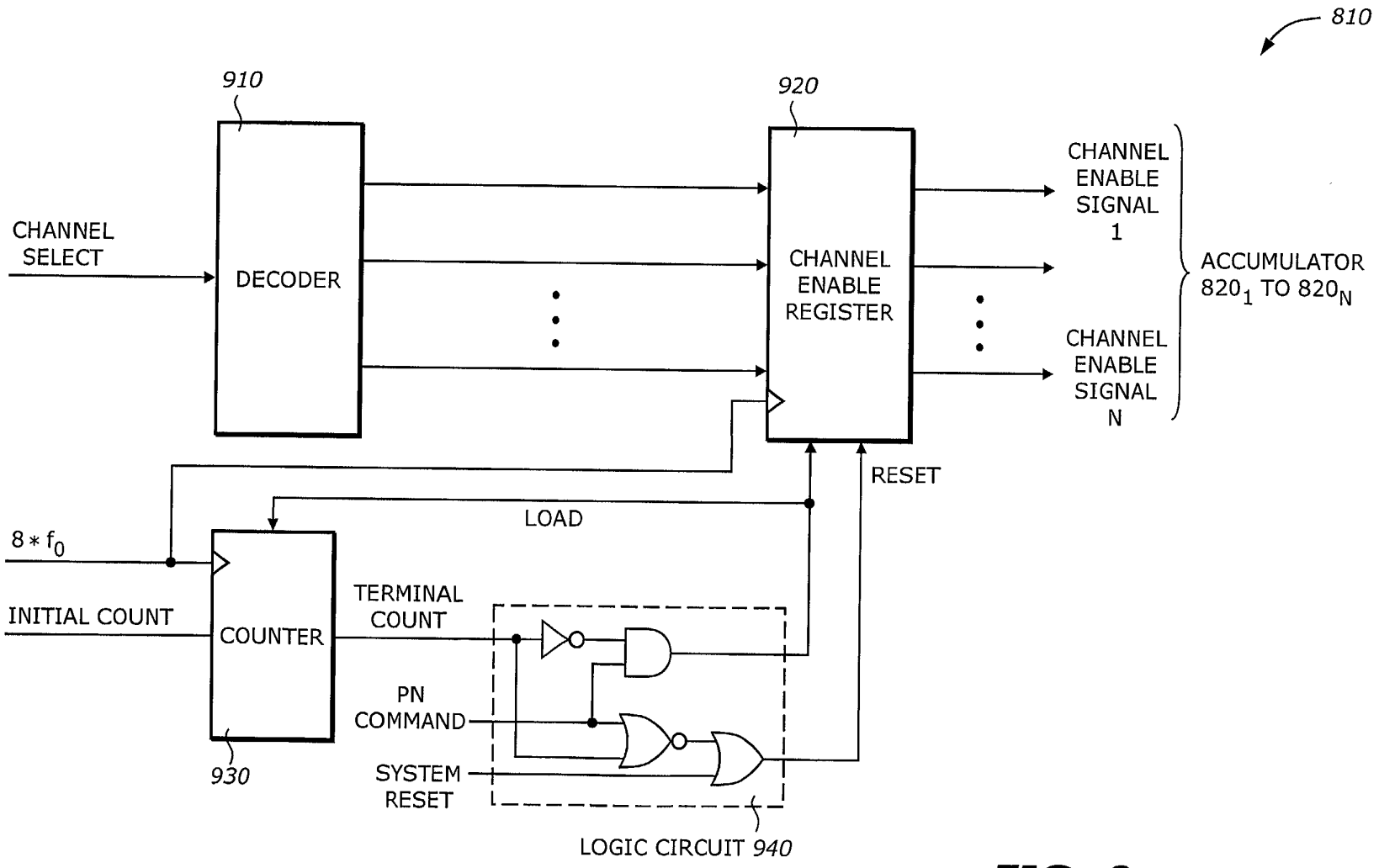
810
910
920
CHANNEL SELECT
DECODER
CHANNEL ENABLE REGISTER
CHANNEL ENABLE SIGNAL 1
CHANNEL ENABLE SIGNAL N
ACCUMULATOR 820_1 TO 820_N
RESET
LOAD
$8 * f_0$
INITIAL COUNT
COUNTER
TERMINAL COUNT
PN COMMAND
SYSTEM RESET
930
LOGIC CIRCUIT 940

FIG. 9

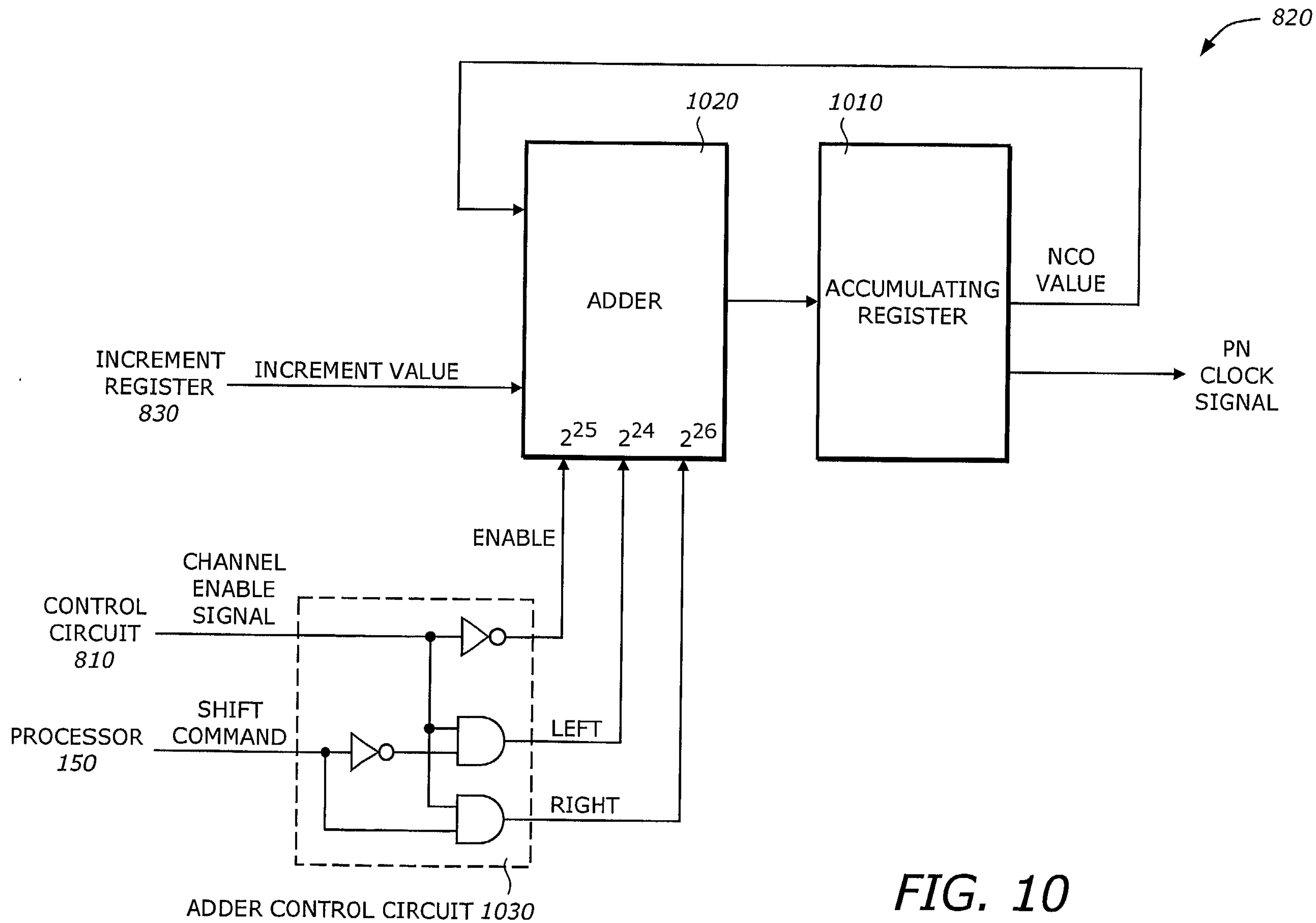
820
1020
1010
ADDER
ACCUMULATING
REGISTER
NCO
VALUE
PN
CLOCK
SIGNAL
INCREMENT
REGISTER
830
INCREMENT VALUE
2^{25} 2^{24} 2^{26}
ENABLE
CHANNEL
ENABLE
SIGNAL
CONTROL
CIRCUIT
810
SHIFT
COMMAND
PROCESSOR
150
LEFT
RIGHT
ADDER CONTROL CIRCUIT 1030

FIG. 10

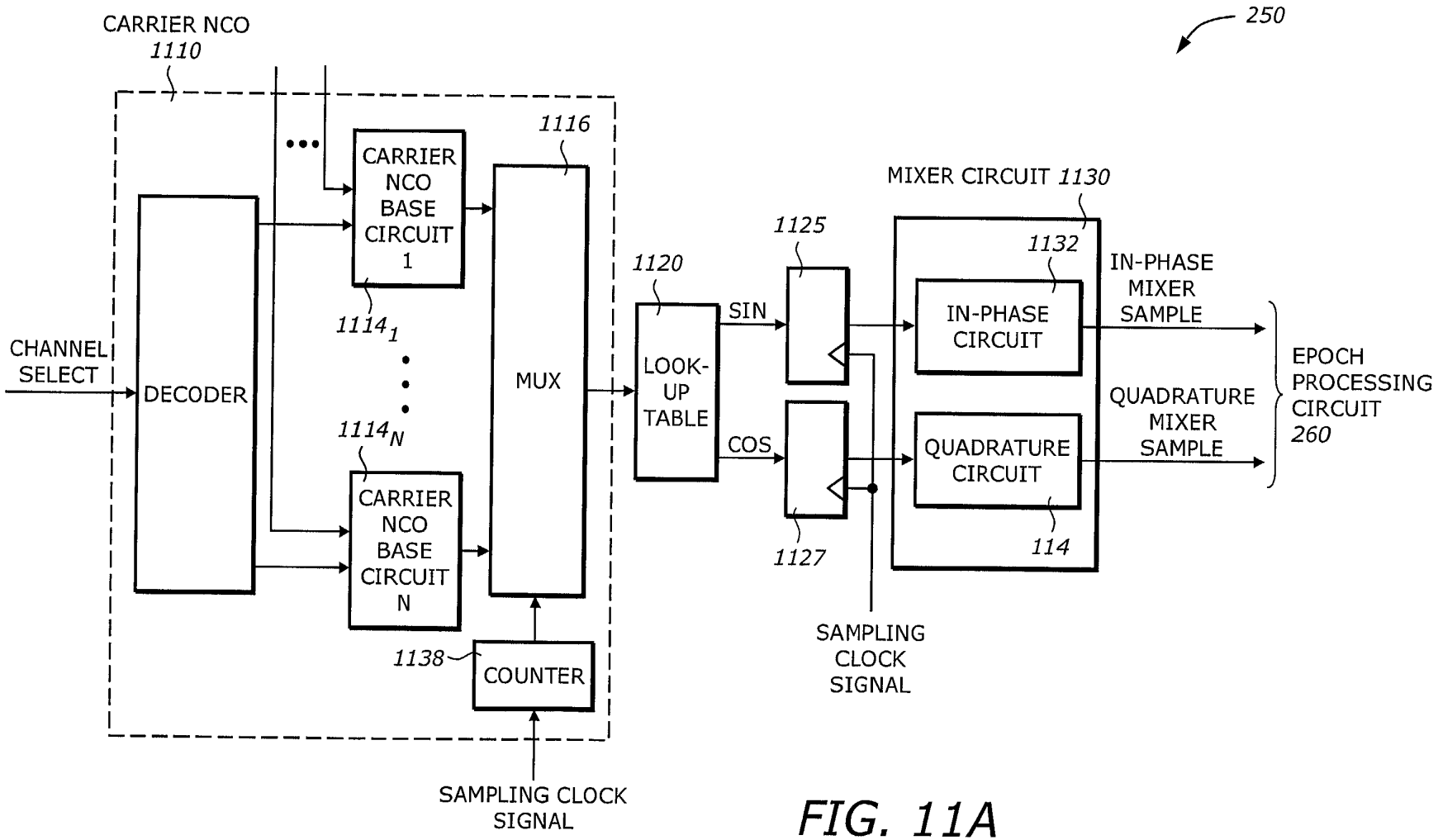
CARRIER NCO
1110
250
1116
CARRIER NCO BASE CIRCUIT 1
1114 1
CHANNEL SELECT
DECODER
MUX
1114 N
CARRIER NCO BASE CIRCUIT N
1138
COUNTER
SAMPLING CLOCK SIGNAL
1120
LOOK-UP TABLE
SIN
COS
1125
1127
MIXER CIRCUIT 1130
1132
IN-PHASE CIRCUIT
QUADRATURE CIRCUIT
114
IN-PHASE MIXER SAMPLE
QUADRATURE MIXER SAMPLE
EPOCH PROCESSING CIRCUIT 260
SAMPLING CLOCK SIGNAL

FIG. 11A

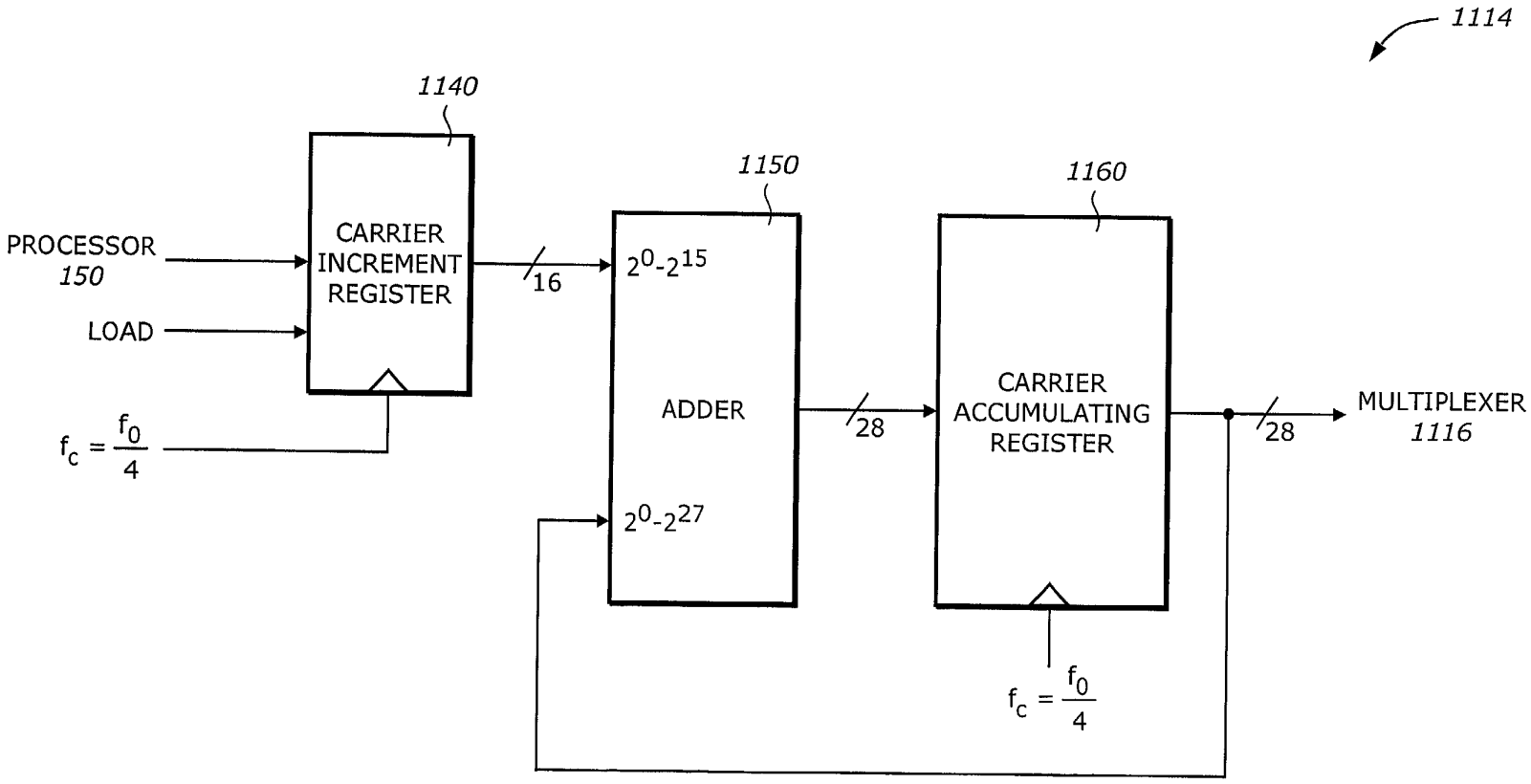

FIG. 11B

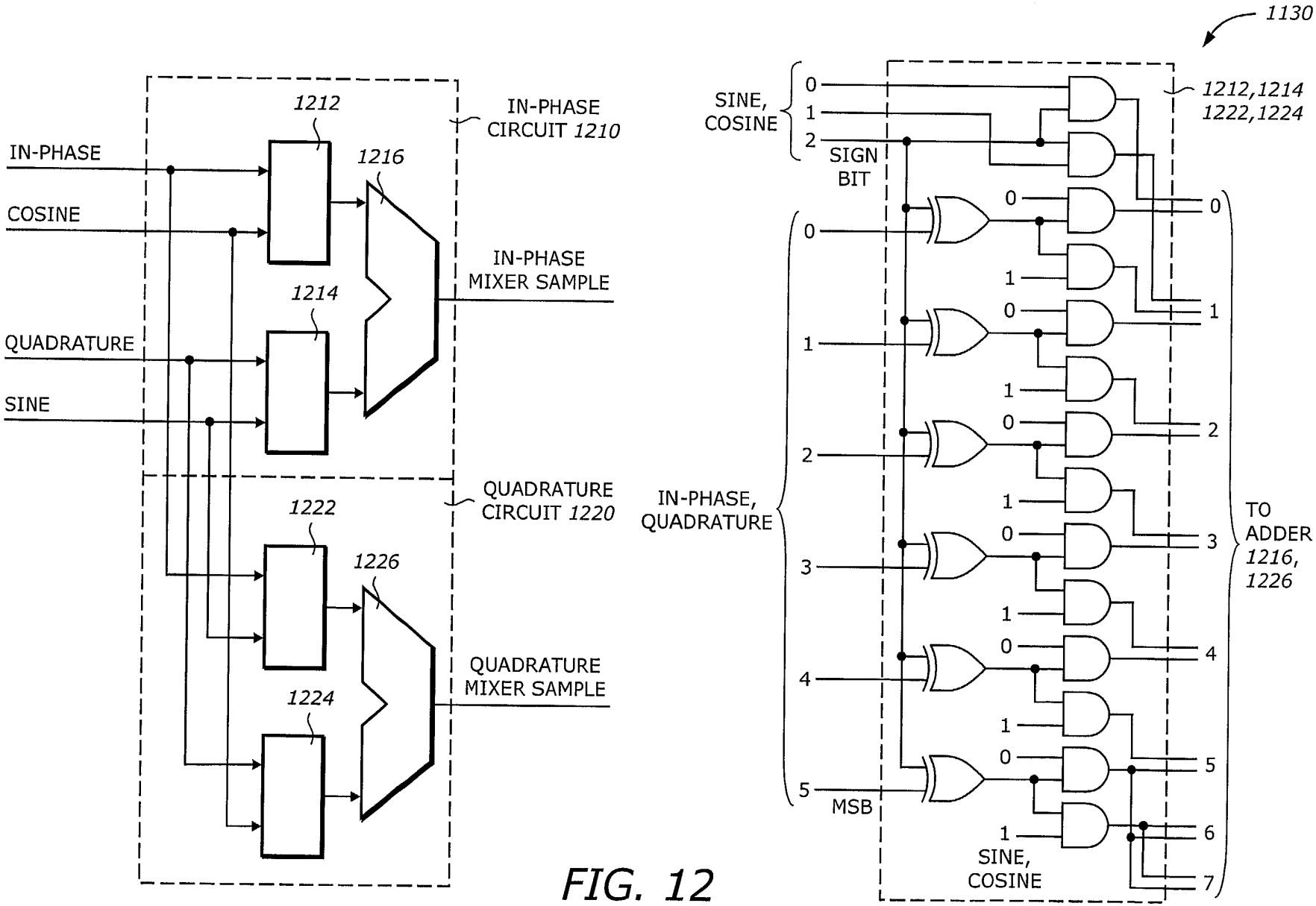

FIG. 12

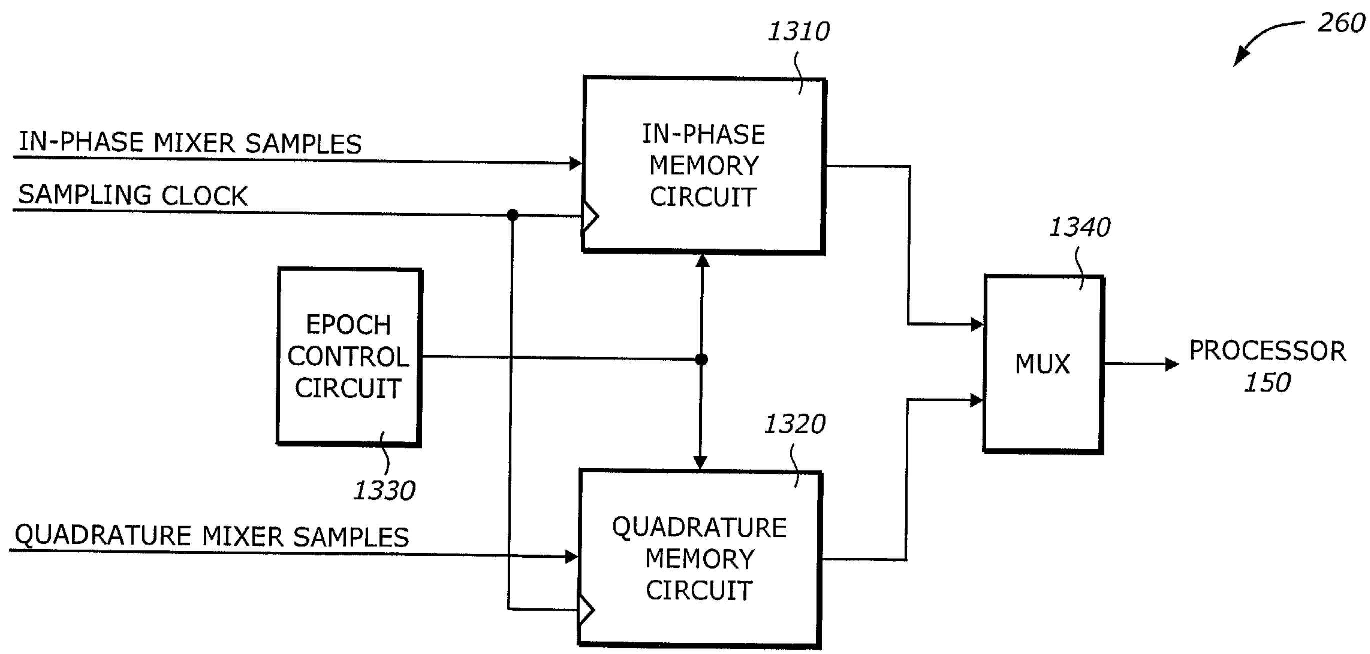
260
1310
IN-PHASE MIXER SAMPLES
SAMPLING CLOCK
IN-PHASE MEMORY CIRCUIT
EPOCH CONTROL CIRCUIT
1330
1320
QUADRATURE MIXER SAMPLES
QUADRATURE MEMORY CIRCUIT
1340
MUX
PROCESSOR 150

FIG. 13

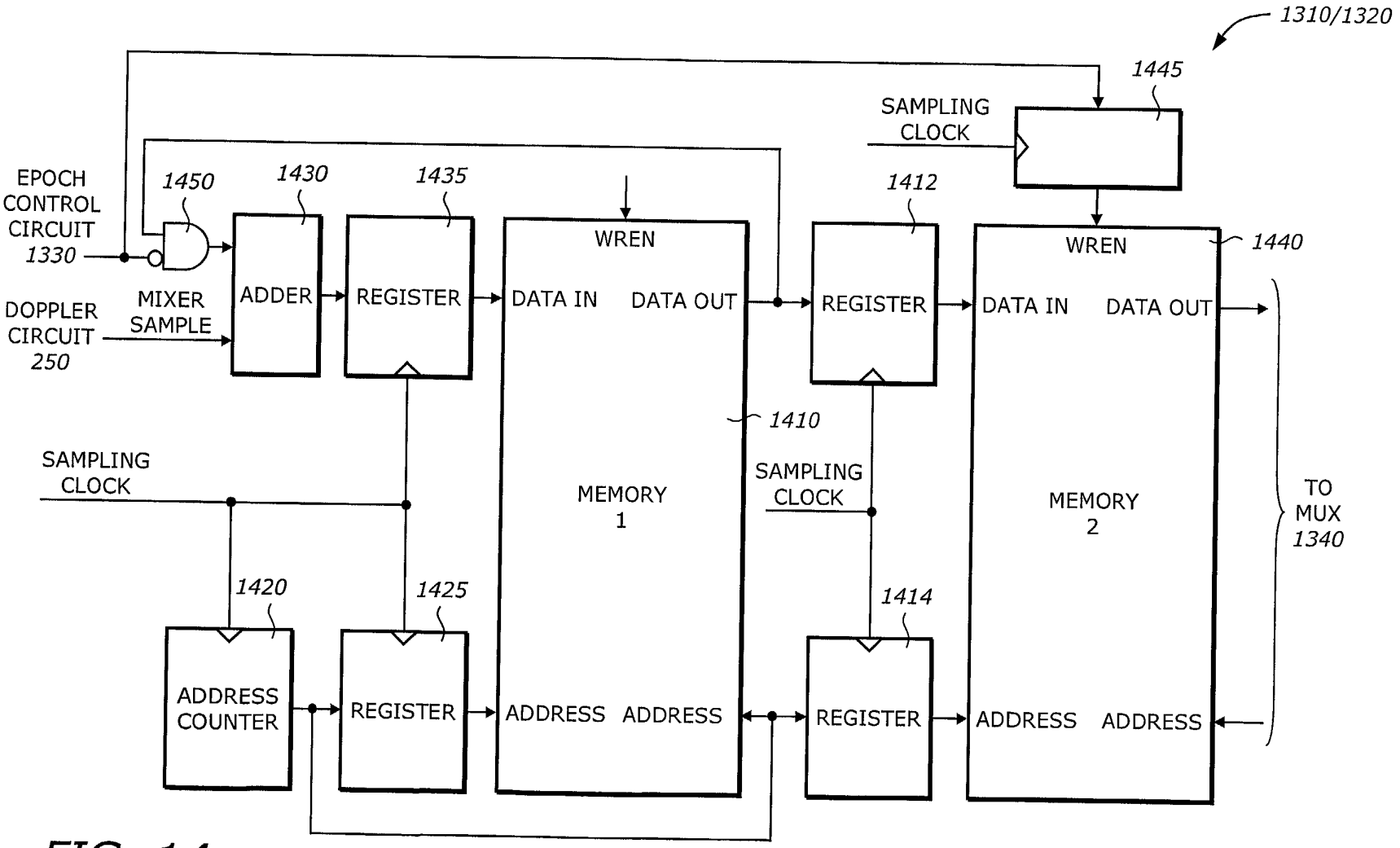

FIG. 14